

REMARKS

Claims 1 - 4 and 6 - 10 remain active in this application. The specification has been reviewed and editorial revisions made where seen to be appropriate. Claims 1, 3, 6 and 7 have been amended to improve clarity. Claim 5 has been canceled and the salient recitations thereof included in claim 1. Support for the amendments of the claims is found throughout the application. No new matter has been introduced into the application. The acknowledgment of the claim for foreign priority, receipt of supporting certified copy of the priority document and consideration of the two Information Disclosure Statements is noted with appreciation.

The Examiner has objected to the drawings as not showing sufficient detail for the invention to be easily understood. This objection is respectfully traversed and moot in view of the proposed drawing revisions submitted herewith.

The Examiner notes the provision of 37 C.F.R. §1.83 which allows schematic representation of structure which is not required for conveying an adequate understanding of the invention but notes that legends should be provided to make the drawings more self-explanatory. It is respectfully submitted, in this regard, that the drawings, as filed, illustrate the architecture embodied by the invention is copious detail and that illustration of details of the structures schematically depicted is not important or necessary to an understanding of the invention. Therefore it is respectfully submitted that the *degree of detail* in the originally filed drawings cannot properly form the basis of an objection. However, the Examiner's observation that the original drawings may not facilitate an understanding of the invention without detailed reference to the specification is

well-taken and the proposed drawing revisions supply numerous legends from the text of the specification to facilitate an understanding of the invention. Since the legends are drawn directly from the specification, no new matter is included in the proposed drawing revisions while the legends provide substantial self-explanatory content to the drawings. Therefore, it is respectfully requested that the proposed drawing revisions be approved. Upon the Examiner's approval of the proposed revisions, correspondingly revised formal drawings will be submitted.

The Examiner has indicated that the lengthy specification has not been reviewed to determine errors therein and requires that any error found be corrected. In response, the specification has been reviewed and editorial revisions made where seen to be appropriate. If the Examiner becomes aware of any other points at which similar revision would be beneficial, it is respectfully requested that the same be pointed out to facilitate similar revision being made.

The Examiner has objected to the specification as failing to provide antecedent identification of the groups recited in claims 6 - 10. The Examiner indicates that the groups can be identified through deduction and no enablement issue is presented. In response, some clarifying amendments have been made to claims 6 - 10. Indeed, it is respectfully submitted that the recitations of groups of instructions in claims 6 - 10 reflect relationships of instructions in respective groups which and refer to the logical order in which the instructions are executed (or not) in dependence on those relationships. Therefore, it is respectfully submitted that the above clarifying amendments to these claims are a full and sufficient response to the Examiner's objection and reconsideration and withdrawal of the same is respectfully requested.

The Examiner has also objected to the Title of the application. This objection is also respectfully traversed as being moot in view of the amendments made above in which a Title very similar to that suggested by the Examiner has been adopted. Accordingly, reconsideration and withdrawal of this ground of objection is also respectfully requested.

The Examiner has objected to the claims because of usage of the phrases "high entry order" and "low entry order" in claim 1 are comparative and thus indefinite and "highest in order" which might be considered as contrary to the specification. This objection is respectfully traversed in view of the amendments made above where the language of claim 1 has been revised and the "order" of claims 6 and 7 has been defined as referring to "priority" and corresponding to a lower entry number, consistent with the specification. Accordingly, reconsideration and withdrawal of this ground of objection is respectfully requested.

Claims 5 and 7 - 10 have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite; generally regarding matters of antecedent language correspondence. This rejection is respectfully traversed as being moot in view of the amendments made above which clarify the points raised by the Examiner and generally adopt language consistent with the Examiner's expressed understanding of the claimed subject matter. Accordingly, reconsideration and withdrawal of this ground of rejection is respectfully requested.

Claims 1 - 10 have been rejected under 35 U.S.C. §102 as being anticipated by Rupley, II, et al. (hereinafter "Rupley"). This ground of rejection is respectfully traversed as being moot in view of the amendments made above.

The present invention is directed to an instruction buffer and a method for controlling an

instruction buffer, particularly for a processor having a pipelined architecture such that several instructions can be processed simultaneously, either in-order or out-of-order. For this purpose, the invention includes two (parallel) instruction registers in which instructions may be stored in order of priority of execution and through which dependencies (e.g. where the execution of one instruction must be deferred until the completion of another instruction) and readiness for execution may be expressed, preferably through a validity bit and dependence and release control fields (68, 69, 88, 89). Thus the instruction registers 22, 23 of the invention can function to deliver instructions in-order or out-of-order in accordance with dependencies while the respective buffers function in a first-in-first-out (FIFO) manner to prevent the instruction buffer(s) from becoming filled with instructions awaiting execution; a condition which slows overall processing.

In contrast, Rupley is concerned with branch prediction, particularly when the outcome a plurality of interrelated or nested branching operations are to be performed. While Rupley provides separate but serially connected instruction and completion unit buffers respectively preceding and following a dispatch unit and execution unit; the latter completion unit being controlled by a branch prediction unit which can invalidate operations including other branch instructions in the completion unit when a branch prediction fails. Thus, while the system of Rupley appears to include a processor having a pipeline architecture and the instruction buffer 20 (but not completion unit 24 since it provides for removal of instructions corresponding to incorrect branch predictions) functions as a FIFO buffer, the remainder of the function of the claimed subject matter and its organization is very different from that of Rupley.

Specifically, in claim 1, Rupley clearly does not answer the recitation of first and second buffers wherein each issues instructions in storage entry order. Rupley does not provide for each entry to indicate whether or not it is ready to be issued as recited in claim 2, observing priority among instructions ready to be issued as recited in claim 3 or providing priority among entries having instruction to entries not having instructions. There is no teaching or suggestion in Rupley of grouping of instructions with logical operations being performed in regard to issuance of instructions in accordance with the group(s) to which a given instruction belongs as recited in claims 7 and 8, the concurrent execution of instructions from different groups as recited in claim 9 or the differentiation, between groups, of memory access instructions and operation instructions as recited in claim 10.

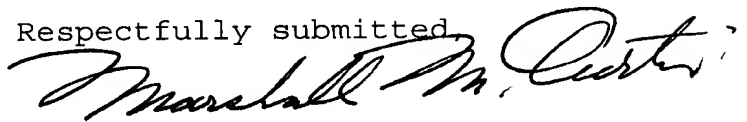
Therefore, it is respectfully submitted that Rupley does not anticipate any claim in the application and the ground of rejection based on Rupley is untenable in regard to the claims as now amended. In addition, it is respectfully pointed out that the Examiner has not made a *prima facie* demonstration of anticipation of the subject matter of at least original claims 2 - 10. Accordingly, it is respectfully requested that the ground of rejection based on Rupley be reconsidered and withdrawn and the application be passed to issue.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that

this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,



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